CLAIMS

Please amend the claims as follows:

1. (amended) A shared memory computer ~~data processing~~ system, comprising:

a plurality of processing nodes connected to operate in a high speed, high bandwidth system interconnect topology;

each of the processing nodes having at least one processor ~~agent~~ therein that executes software instructions to process data;

volatile memory distributed in one or more of said processing nodes providing data and instruction storage in a shared memory address space accessible to multiple of said plurality of processing nodes through communication via said high speed system interconnect;

a recovery bus ~~in the system topology~~ operating at a lower speed than the high speed topology and connecting the plurality of processing nodes together;

cache coherency circuitry snooping communication on the high speed system interconnect topology to maintain cache coherency in said distributed volatile memory;

~~the~~ agents in the processing nodes monitoring ~~the status of processing in~~ the high speed interconnect topology to sense an ~~a system~~ error therein ~~the high speed topology~~; and

the agents in the processing nodes transferring communication from the high speed interconnect topology to the recovery bus in response to sensing an ~~a system~~ error in the high speed interconnect topology.

2. (amended) The shared memory computer ~~data processing~~ system of claim 1, wherein the high speed system interconnect topology is a non-hierarchical loop interconnect architecture.

3. (amended) The shared memory computer ~~data processing~~ system of claim 1, wherein the high speed system interconnect topology is a hierarchical bus topology.

4. (amended) The shared memory computer ~~data processing~~ system of claim 1, further including:

the agents in the processing nodes transferring communication from the recovery bus to the high speed interconnect topology in response to the ~~system~~ error being remedied.

5. (amended) The shared memory computer ~~data processing~~ system of claim 1, wherein the recovery bus is a wired bus.

6. (amended) The shared memory computer ~~data processing~~ system of claim 1, wherein the recovery bus is a virtual bus.

7. (amended) The shared memory computer ~~data processing~~ system of claim 2, wherein the high speed system interconnect topology includes:

a plurality of address channels coupling said plurality of nodes, wherein each agent in all of said plurality of nodes is coupled to all of said plurality of address channels, and wherein each agent can issue transactions on only a single associated address channel among said plurality of address channels and snoops transactions on all of said plurality of address channels; and

at least one data channel coupling said plurality of nodes~~; and~~

~~data storage accessible to agents within said plurality of nodes~~.

8. (amended) The shared memory computer ~~data processing~~ system of claim 7, wherein said plurality of address channels comprises a plurality of address buses.

9. (amended) An interconnect system for a computer ~~data processing~~ system~~, said data processing system~~ including a plurality of processing nodes that each include at least one processing unit for executing software instructions to process data ~~agent~~, said interconnect system comprising:

a high speed, high bandwidth interconnect~~ion~~ topology connecting the plurality of processing nodes within the computer system and conveying, between the plurality of processing nodes, requests of processing units for data residing within a shared memory distributed among said plurality of processing nodes and associated cache coherency communication;

a recovery bus in the system topology operating at a lower speed than the high speed interconnect topology and connecting the plurality of processing nodes together; and

means for transferring communication directed from one processing node to another processing node in the computer system from the high speed topology to the recovery bus in response to a system error in the high speed topology.

10. (original) The interconnect system of claim 9, wherein the recovery bus is a wired bus.

11. (original) The interconnect system of claim 9, wherein the recovery bus is a virtual bus.

12. (amended) The interconnect system of claim 9, wherein the high speed system interconnect topology includes:

a plurality of address channels coupling said plurality of processing nodes, wherein each agent in all of said plurality of nodes is coupled to all of said plurality of address channels, and wherein each agent can issue transactions on only a single associated address channel among said plurality of address channels and snoops transactions on all of said plurality of address channels; and

at least one data channel coupling said plurality of nodes~~; and~~

~~data storage accessible to agents within said plurality of nodes~~.

13. (original) The interconnect system of claim 12, wherein said plurality of address channels comprises a plurality of address buses.

14. (amended) A method of communication in a shared memory computer ~~data processing~~ system having a plurality of processing nodes that each include at least one processor that executes software instructions to process data ~~agent~~, said method comprising:

coupling the plurality of nodes together to operate ~~operating~~ in a high speed, high bandwidth interconnect topology;

utilizing communication on the high speed interconnect topology, accessing distributed volatile memory in one or more of said processing nodes that provides data and instruction storage in a shared memory address space accessible to multiple of said plurality of processing nodes;

utilizing communication on the high speed interconnect topology, maintaining cache coherency within said distributed volatile memory;

providing a recovery bus in the high speed system topology that operates ~~and operating~~ at a lower speed than the high speed interconnect topology;

monitoring the ~~status of processing in~~ ~~the~~ high speed interconnect topology to sense an ~~system~~ error in the high speed interconnect topology; and

transferring communication from the high speed interconnect topology to the recovery bus in response to sensing an ~~system~~ error in the high speed interconnect topology.

15. (amended) The method of claim 14, further including the step of:

transferring communication from the recovery bus to the high speed interconnect topology in response to the ~~system~~ error being remedied.

16. (original) The method of claim 14, wherein said step of coupling comprises steps of:

coupling at least one data channel to said plurality of nodes;

coupling each agent in all of said plurality of nodes to each of a plurality of address channels;

permitting each agent to issue transactions on only a single associated address channel; and

snooping, with each agent, transactions on all of said plurality of address channels.

17. (original) The method of claim 16, wherein said plurality of address channels comprises a plurality of address buses, and wherein permitting each agent to issue transactions on only a single associated address channel comprises permitting each agent to issue transactions on only an address bus associated with its node.

18. (original) The method of claim 16, wherein coupling at least one data channel to said plurality of nodes comprises coupling to all of said plurality of nodes only a single data channel.

19. (original) The method of claim 16, wherein said coupling steps comprise coupling each agent in said plurality of nodes to a switched interconnect.

20. (amended) The method of claim 16, ~~said data processing system comprising data storage distributed among said plurality of nodes,~~ wherein said permitting step comprises permitting each agent to issue requests for data within said volatile memory ~~distributed data storage~~ on only an address channel associated with its node.

21. (original) The method of claim 16, said data processing system including response logic at each node, said method farther comprising:

in response to snooping a transaction on one of said plurality of address channels, providing a snoop response from each agent at a node to response logic at that node; and

combining said snoop response of each agent at that node to produce a combined response for that node.

22. (original) The method of Claim 21, said combining step further comprising combining said snoop, response of each agents at that node with a combined response received from another of said plurality of nodes to produce said combined response.

23. (newly entered) The shared memory computer system of Claim 1, wherein:

said volatile memory includes cache memory in at least a particular node among said plurality of nodes; and

said particular node includes response logic providing cache coherency responses to communication transactions snooped on the high speed interconnect topology and the recovery bus.

24. (newly entered) The interconnect system of Claim 9, wherein said computer system includes cache memory in at least a particular node among said plurality of nodes, and wherein said interconnect system includes response logic providing cache coherency responses to communication transactions snooped on the high speed interconnect topology and the recovery bus.

25. (newly entered) The method of Claim 14, wherein said volatile memory includes cache memory in at least a particular node among said plurality of nodes, and wherein said method further comprises response logic in said particular node providing cache coherency responses to communication transactions snooped on the high speed interconnect topology and the recovery bus.